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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/652,028	09/02/2003	Takahiro Fujioka	HITA.0426	1544

38327 7590 12/15/2005

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EXAMINER	
KUMAR, SRILAKSHMI K	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/652,028	FUJIOKA ET AL.	
	Examiner	Art Unit	
	Srilakshmi K. Kumar	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-10 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-10 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/836,339.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/03 & 3/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-10 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-15 of U.S. Patent No. 6,862,015. Although the conflicting claims are not identical, they are not patentably distinct from each other as will be shown in the table below.

Instant Application 10/652,028 Claim 1	US Patent 6,862,015 Claim 1
A liquid crystal display device having a liquid crystal display panel, a plurality of liquid crystal circuits formed over an edge portion of the liquid crystal display panel, and a plurality of signal lines formed over the edge portion of the liquid crystal display panel for transmitting an image signal and an external clock signal between respective drive circuits, wherein the liquid crystal drive circuit comprises;	A liquid crystal display device having a liquid crystal display panel, a plurality of cascade-connected liquid crystal drive circuits for sequentially transferring a signal, and a plurality of signal lines formed over an edge portion of the liquid crystal display panel for transmitting a signal between any two of the drive circuits, wherein each of the liquid crystal drive circuits comprises;
An image signal input circuit connected with	An image input terminal connected with one of

the signal line;	the signal lines to receive an external image signal being input thereto as an internal image signal into said each of the liquid crystal drive circuits;
A clock control circuit connected with the signal line, and generating an internal clock signal based on the external clock signal; Having a clock compensation circuit;	A clock input terminal connected with another one of the signal lines to receive an external clock signal being input thereto; a clock compensation circuit for generating an internal clock signal based on the external clock signal;
The internal clock signal swinging from a first voltage to a second voltage lower than the first voltage;	Said internal clock signal swinging from a first voltage to a second voltage lower than the first voltage;
A data storage circuit for storing an image signal at a timing of a voltage changing from a first voltage to a second voltage or at a timing of a voltage changing from a second voltage to a first voltage of the internal clock signal;	A data storage circuit for storing therein the internal image signal at a timing of a voltage change from the first voltage to the second voltage as a first image signal and at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal as a second image signal
A voltage select circuit for selecting a voltage for driving the liquid crystal display panel;	A voltage select circuit for selecting a voltage according with the first and second image signals to drive the liquid display panel
An output circuit for outputting the external clock signal to next liquid crystal drive circuit.	A clock signal output circuit for outputting the internal clock signal as a subsequent external clock signal;

The above table discloses the similarities in claim 1 of the instant application with that of the US Patent 6,862,015. The claims are not patentably distinct from each other as the changes in the some of the claim language does not change the functionality of the invention.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4-6, 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Someya et al (US 5,091,784) in view of Sasaki et al (US 6,211,849).

As to independent **claim 1**, Someya et al disclose a liquid crystal display device having a liquid crystal display panel, a plurality of liquid crystal circuits formed over an edge portion of the liquid crystal display panel (Fig. 2), and a plurality of signal lines formed over the edge portion of the liquid crystal display panel for transmitting an image signal (Fig. 2) and an external clock signal between respective drive circuits (Fig. 2), wherein the liquid crystal drive circuit comprises; an image signal input circuit connected with the signal line (col. 5, lines 30-59); a clock control circuit connected with the signal line (input into Fig. 2, item 8, clock generator), and generating an internal clock signal based on the external clock signal. (col. 6, line 61-col. 7, line 5 and col. 7, lines 41-52); the internal clock signal swinging from a first voltage to a second voltage lower than the first voltage (col. 7, lines 41-52); a data storage circuit for storing an image signal at a timing of a voltage changing from a first voltage to a second voltage or at a timing of a voltage changing from a second voltage to a first voltage of the internal clock signal (Fig. 2, item 25, col. 7, lines 41-52); a voltage select circuit for selecting a voltage for driving the liquid crystal display panel (col. 10, lines 15-50); having a clock compensation circuit (Fig. 2, item 8);

Someya et al do not disclose an output circuit for outputting the external clock signal to next liquid crystal drive circuit. Sasaki et al disclose in Figs. 4 and 5 and col. 4, lines 46-67, col. 5, lines 5-12, 30-41, a clock signal output circuit where the internal clock signal is output to subsequent liquid crystal drive circuit. It would have been obvious to one of ordinary skill in the art to incorporate the feature of outputting the external clock signal to the next liquid crystal drive circuit as shown by Sasaki in to the system of Someya et al as the clock signal output circuit enables a liquid crystal display device of achieving higher resolution by regulating the duty cycle ratio as is disclosed by Sasaki in col. 2, line 25-col. 3, line 3.

As to independent **claim 6**, Someya et al disclose a liquid crystal display device having a liquid crystal display panel, a plurality of liquid crystal circuits formed over an edge portion of the liquid crystal display panel (Fig. 2), and a plurality of signal lines formed over the edge portion of the liquid crystal display panel for transmitting an image signal (Fig. 2), wherein the liquid crystal drive circuit comprises: a data input terminal connected with the signal line, and an image signal being input thereto (col. 5, lines 30-59); a clock control circuit for inputting an external clock and outputting an internal clock (input into Fig. 2, item 8), the internal clock having a first period for permitting output of a first voltage and a second period for output of a second voltage (col. 7, lines 41-52); a data latch circuit for taking thereto an image signal at a timing of a voltage changing from a first voltage to a second voltage or at a timing of a voltage changing from a second voltage to a first voltage of the internal clock (Fig. 2, item 25, col. 7, lines 41-52); a data bus for output of the image signal from the data latch circuit (col. 10, lines 15-50); and a clock formation circuit being operable to correct a duty ratio of the external clock (col. 6, line 61-col. 7, line 5, 41-52); a voltage output circuit for outputting a voltage according to

the image signal on the data bus to the liquid crystal display element (Fig. 15, item 107, col. 13, lines 11-18);

Someya et al do not disclose a data output circuit for outputting the image signal on the data bus to a next stage of liquid crystal drive circuit. Sasaki et al disclose in Figs. 4 and 5 and col. 4, lines 46-67, col. 5, lines 5-12, 30-41, a data output circuit for outputting the image signal on the data bus to a next stage of liquid crystal drive circuit. It would have been obvious to one of ordinary skill in the art to incorporate the feature of outputting the data signal to the next liquid crystal drive circuit as shown by Sasaki in to the system of Someya et al as the data output circuit enables a liquid crystal display device of achieving higher resolution by regulating the duty cycle ratio as is disclosed by Sasaki in col. 2, line 25-col. 3, line 3.

As to dependent **claim 2**, limitations of claim 1, and further comprising, Someya et al do not disclose wherein the clock compensation circuit is operable to correct a duty ratio of the external clock.

Sasaki et al disclose in Figs. 4 and 5 and col. 4, lines 46-67, col. 5, lines 5-12, 30-41, wherein the clock compensation circuit is operable to correct a duty ratio of the external clock. It would have been obvious to one of ordinary skill in the art to incorporate the feature of correcting a duty ratio of the external clock as shown by Sasaki in to the system of Someya et al as regulating the duty cycle ration enables a liquid crystal display device of achieving higher resolution as is disclosed by Sasaki in col. 2, line 25-col. 3, line 3.

As to dependent **claim 4**, limitations of claim 1, and further comprising, Someya et al disclose wherein the clock compensation circuit has a phase locked loop circuit (Fig. 31, item 121).

As to dependent **claim 5**, limitations of claim 1, and further comprising, Someya et al do not disclose wherein the clock compensation circuit has a delay locked loop circuit. Sasaki et al disclose wherein the clock compensation circuit has a delay locked loop circuit in col. 5, line 56-col. 6, line 9. It would have been obvious to one of ordinary skill in the art to incorporate the feature of delay locked loop circuit as shown by Sasaki in to the system of Someya et al as the delay locked loop circuit enables a liquid crystal display device of achieving higher resolution by regulating the duty cycle ratio and phase shifting as is disclosed by Sasaki in col. 2, line 25-col. 3, line 3.

As to dependent **claim 8**, limitations of claim 6, and further comprising, wherein the clock formation circuit has a phase locked loop circuit (Fig. 31, item 121).

As to dependent **claim 9**, limitations of claim 6, and further comprising, Someya et al do not disclose wherein the clock formation circuit has a delay locked loop circuit. Sasaki et al disclose wherein the clock formation circuit has a delay locked loop circuit in col. 5, line 56-col. 6, line 9. It would have been obvious to one of ordinary skill in the art to incorporate the feature of delay locked loop circuit as shown by Sasaki in to the system of Someya et al as the delay locked loop circuit enables a liquid crystal display device of achieving higher resolution by regulating the duty cycle ratio and phase shifting as is disclosed by Sasaki in col. 2, line 25-col. 3, line 3.

As to dependent **claim 10**, limitations of claim 6, and further comprising, Someya et al disclose wherein the data bus comprises two systems of signal lines (Fig. 2, input from sample hold circuit and terminal 29.

5. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Someya et al and Sasaki et al as applied to claims 1 and 6 above, and further in view of Murata et al (US 6,144,355).

As to dependent **claim 3**, limitations of claim 1, and further comprising, Someya et al and Sasaki et al do not disclose wherein the clock compensation circuit has an inverter. Murata et al discloses a clock compensation circuit comprising an inverter in col. 5, lines 41-67, Fig. 1, items 9 and 56. It would have obvious to one of ordinary skill in the art to incorporate the inverter into the clock compensation circuit as shown by Murata et al, as the clock compensation circuit shown by Murata et al enables higher operation speed to attain high precision, accurate image data sampling to achieve enhanced quality in displayed images as disclosed in col. 3, lines 42-60 of Murata et al.

As to dependent **claim 7**, limitations of claim 6, and further comprising, Someya et al and Sasaki et al do not disclose wherein the clock formation circuit has an inverter. Murata et al discloses a clock formation circuit comprising an inverter in col. 5, lines 41-67, Fig. 1, items 9 and 56. It would have obvious to one of ordinary skill in the art to incorporate the inverter into the clock formation circuit as shown by Murata et al, as the clock formation circuit shown by Murata et al enables higher operation speed to attain high precision, accurate image data sampling to achieve enhanced quality in displayed images as disclosed in col. 3, lines 42-60 of Murata et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 571 272 7769. The examiner can normally be reached on 10:00 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571 272 3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Srilakshmi K. Kumar
Examiner
Art Unit 2675

SKK
December 9, 2005

KENT CHANG
PRIMARY EXAMINER